



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,914	03/03/2004	Lcc-Yin Chee	PJW190	3848

7590 09/07/2007
Paul J. Winters
307 Cypress Point Drive
Mountain View, CA 94043

EXAMINER

CEHIC, KENAN

ART UNIT	PAPER NUMBER
----------	--------------

2609

MAIL DATE	DELIVERY MODE
-----------	---------------

09/07/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/791,914

Applicant(s)

CHEE ET AL.

Examiner

Kenan Cehic

Art Unit

2609

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For the claim limitation "the second value" in claim 3, line 2, it is not clear if applicant is referring to "a second state" in claim 1 line 3 or if it is a first occurrence of a new claim limitation.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1, 3 and 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Tateishi (US 5,383,177).

For claim 1, Tateishi teaches method for use in verification of a device (see Fig. 11- 12) comprising :
providing a plurality of packet classes (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502; different packets/payloads can be generated);
providing a flag (see Figure 12, reference 503 when; in this disposal flag can be set or not set) , which may be of a first or a second state (see Figure 12, reference 504 and column 13 lines 9-11; it is inherent that a bit is either 0 or 1), for each of the plurality of packet classes (see column 9 lines

Art Unit: 2609

26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, and column 12 lines 50-53; different packets/payloads can be generated);

generating a packet (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, also Figure 12, reference 505 & 506, column 12 lines 50-53, also column 14 lines 9-21; different packets/payloads can be generated);

if the flag of the packet class of the generated packet is in the first state (see Figure 12, reference 503, decision N ; disposal flag is not set), testing the device (See Figure 12, especially 505-512 , column 12 lines 37-39, Figure 6, and column 13 lines 17-20; the packet is sent to the under-test device).

For claim 3, Tateishi teaches if the flag of the packet class of the generated packet is of the second value (see Figure 12, reference 504-506; the disposal flag is set), not testing the device (see Figure 12, 507 and 512; if disposal flag is set to 1 error rate measurement in reference 512 is not performed).

For claim 4, Tateishi teaches A method for use in verification of a device (see Fig. 11- 12) comprising:

providing a plurality of packet classes (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502; different packets/payloads can be generated);

providing a flag (see Figure 12, reference 503 when; in this disposal flag can be set or not set) , which may be of a first or a second state (see Figure 12, reference 504 and column 13 lines 9-11; it is inherent that a bit is either 0 or 1), which may be of a first or a second state (see Figure 12, reference 504 and column 13 lines 9-11; it is inherent that a bit is either 0 or 1), for each of the plurality of packet classes (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, and column 12 lines 50-53; different packets/payloads can be generated);;

Art Unit: 2609

generating a packet (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, also Figure 12, reference 505 & 506, column 12 lines 50-53, also column 14 lines 9-21; different packets/payloads can be generated); if the flag of the packet class of the generated packet is in the second state (see Figure 12, reference 503, decision N ; disposal flag is set to 1), not testing the device (see Figure 12, 507 and 512; if disposal flag is set to 1 error rate measurement in reference 512 is not performed).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

Art Unit: 2609

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi (US 5,383,177) in view of Ramaiah et al. (US 2005/0216954 A1)

For claim 2, Tateishi teaches all the claimed invention as described in the paragraph 4.

For claim 5, Tateishi teaches (a) providing a plurality of packet classes;

(a) providing an injection flag (see Figure 12, reference 504), which may be of a first or a second state (see Figure 12; reference 504 or 503 decision N, disposal flag is either set 1 or not), for each of the plurality of packet classes (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, and column 12 lines 50-53; different packets/payloads can be generated);

(c) generating a packet (see column 9 lines 26-29, column 4 lines 47-50 and figure 12, reference sign 504, 502, also Figure 12, reference 505 & 506, column 12 lines 50-53, also column 14 lines 9-21; different packets/payloads can be generated);

(d) if the injection flag of the packet class of the generated packet is in the second state (see Figure 12, reference 504;),

not testing the device (see Figure 12 reference 504 and decision block 507, and 512; if disposal flag is set to 1 error rate measurement is not performed);

(e) if the injection flag of the packet class of the generated packet is in the first state (see Figure 12, reference 504),

testing the device (see Figure 12, reference 503,507 and 512; error rate measurement is preformed if disposal flag was not set)

For claims 2 and 5, Tateishi teaches the injection flag, the packet classes, the first state, and the generated packet as described above. However, Tateishi does not teaches that the flag is set to the second state when it was in the first state. Ramaiah et al from the same or similar endeavor teaches setting the flag of the packet of the to the second state (see section 0069 lines 7-12). Thus it would have been obvious to a person of ordinary skill in the art to combine of setting the flag from a first state (not set ie. 0 as described in Figure 12 decision No of block 503 of Tateishi et al) to a second state, when the packet was received and range of valid values is present, into the device testing method as described by Tateishi et al. One could have implemented the algorithm as shown in figure 3 of Ramaiah into either the reception section (3e) as taught by Tateishi. One could have implemented a circuit that implements the TCP RST packet in via the packet section, the random packet generator and the method as shown Figure 12 could have been implemented the RST packet. Like in Figure 12, reference 504, one could have set the fixed pattern to implement the RST packet. Similarly one could have implemented the detection circuit which would set the flag to indicate prior receipt. The motivation for claims 2 and 5 is that one can note if the packet was in the range of allowed value. Additionally, to prevent the device under test to stop function/being able to communicate if to many packets (like the RST packets), which cause the device under test to be unable to function properly if packets (which might be generated by the random generator).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tateishi (US 5,383,177) in view of Ramaiah et al. (US 2005/0216954 A1) as applied to claim 5 above, and further in view of Denton et al. (US 2003/0179777 A1).

For claim 6, Tateishi and Ramaiah et al teach all the claimed invention as described in paragraph 8 and additionally the steps c through 3. Tateishi and Ramaiah et al do not teach that certain test steps are repeated. Denton et al from the same or similar field of endeavor teaches repeating test packet generation (see section 0065 lines 23-28).

Thus it would have been obvious to a person of ordinary skill in the art to combine the teaching of repeating test packet generation and testing, as taught by Denton et al., into the method of device testing as taught by Tateishi and Ramaiah et al. One could have implemented this method via an additional counter circuits built into both the transmitting and receiving section of the packet switching testing apparatus as taught by Tateishi in Figure 11. All the components of both section would be synchronized by a clock to produce/receive packets in order to test the device 6, in Figure 11 of Tateishi. The motivation is that one could test/synchronize the device under test so that synchronous operation is present (as suggested by Denton et al. ; see section 0017).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US-2003/0061581 A1	03-2003	Baumgartner et al.
US-2003/0142629 A1	07-2003	Krishnamurthi et al.
US-2004/0223458 A1	11-2004	Gentle, Christopher Reon
US-2006/0209709 A1	09-2006	Kovacevic, Branko D.

Art Unit: 2609

US-2007/0008897 A1	01-2007	Denton et al.
US-2007/0147257 A1	06-2007	Oskouy et al.
US-2007/0168748 A1	07-2007	Musoll, Enrique

The above are recited to show test packet generation and test systems.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenan Cehic whose telephone number is (571) 270-3120. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton can be reached on (571) 272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KC



DANG T. TON
SUPERVISORY PATENT EXAMINER